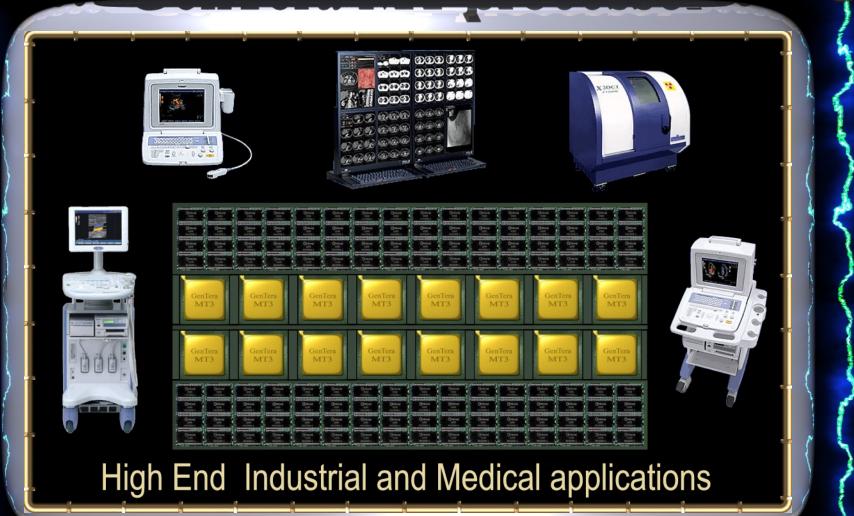
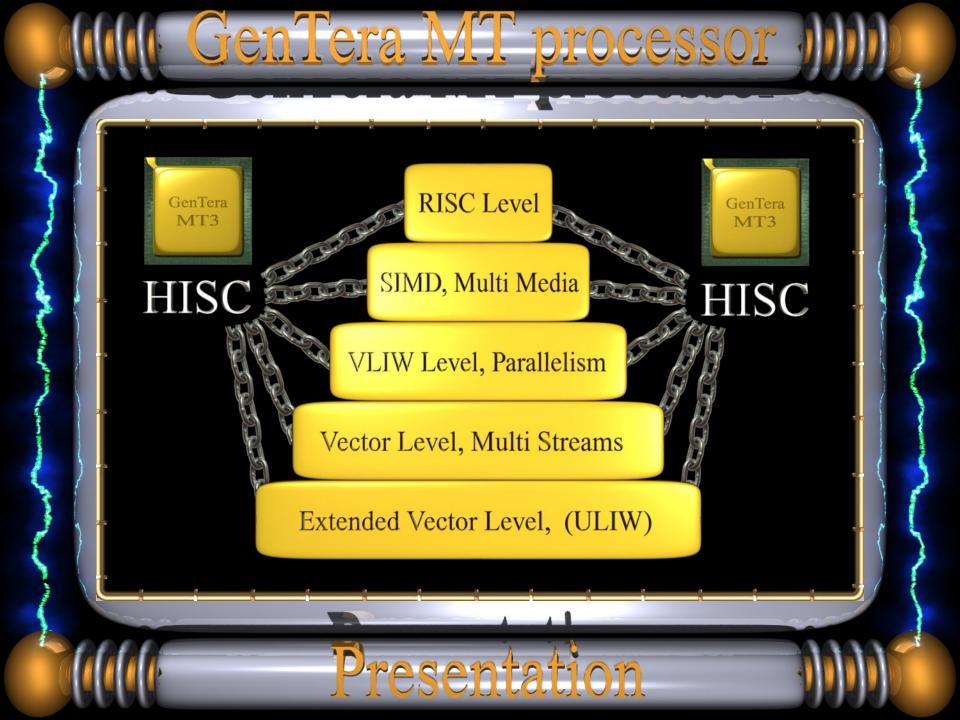




# IIIII GenTera MT processor IIIII





### MT3 Advanced Functionality

Adv. Pipelined Integer, Fractional, **DSP** and **SIMD** operations

Streaming SIMD data & multi media array access

Video codec support functions

routing

On Chip Data, Instr. cache access

Adv. Pipelined Floating Point: + - x /  $\sqrt{\sin \cos \theta}$ In exp asin acos

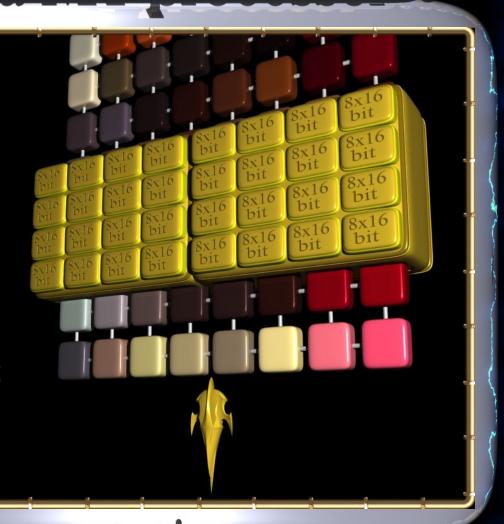
Streaming 3D texture & volume access and preprocessing



# Multi Functional Multipliers

Pixel Processing: 8x8 and 8x16 with 16 bit coeficients and internal vector file.

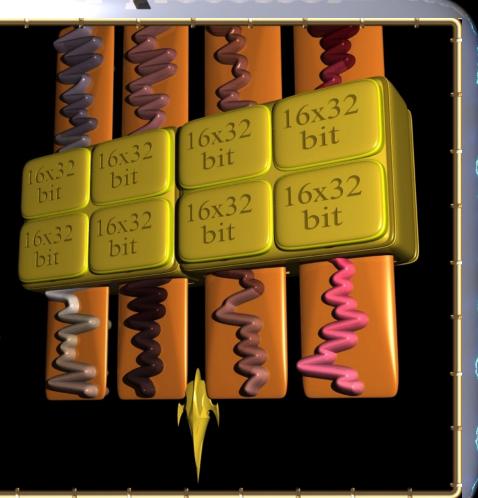
- 4x4 Matrix x Vector
- Quad Vector Inproduct
- Open GL Blending
- (Vector) Accumulation
- Range Clipping



# Multi Functional Multipliers

Audio and Sonar: 16x16 and 16x32 with 32 bit coeficients and internal vector file.

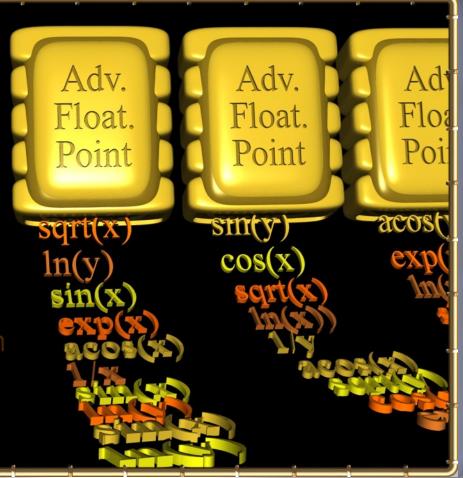
- Dot and Cross Products
- Complex Products
- Quad FIR Filter Stages
- (Vector) Accumulation
- Range Clipping



# Advanced Pipelined Floating Point

Multiple independent Five stage units can produce floating point results each cycle.

- Reciprocal and Sq Root
- Exponent and Logarithm
- Sine and Cosine
- ArcSine and ArcCosine

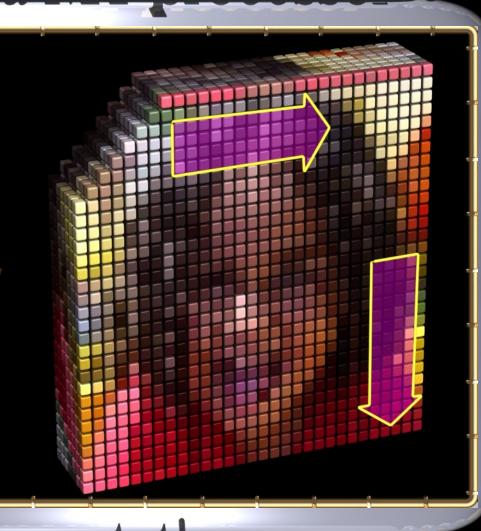


# IIIIII GenTera MT processor

Streaming SIMD data & multi media array access:

Multiple SIMD words per cycle with arbitrary byte address offsets

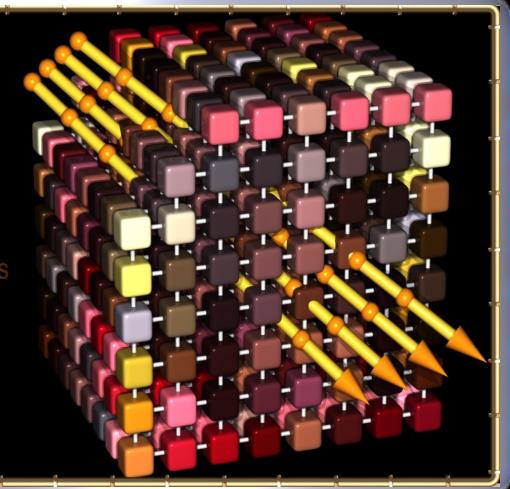
- 1D, 2D and 3D Arrays
- Horizontal / Vertical
- Read and Write



Streaming
Perspective 3D
texture & volume
processing units

Gen. functionality for many applications

- Fully Open GL compatible
- 32, 16 and 8 bit components

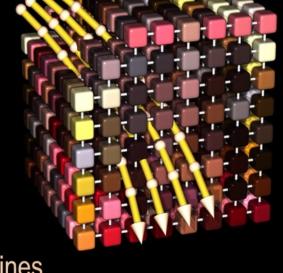


## IIIIII GenTera MT processor

### **Curfed Texture Mapping**

Streaming addresses for the Perspective 3D Texture and Volume units can also come from Advanced Floating Point units or SIMD memory Data

- All Perspective and Lighting operations handled by the 3D pipelines
- All Bi, Tri and Quad Linear interpolations handled by 3D pipelines
- Allows the highest quality graphics without triangle explosion

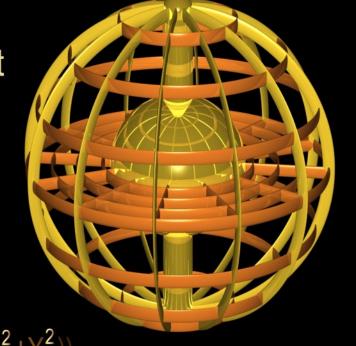




Curfed Texture Mapping & Advanced Floating Point Example:

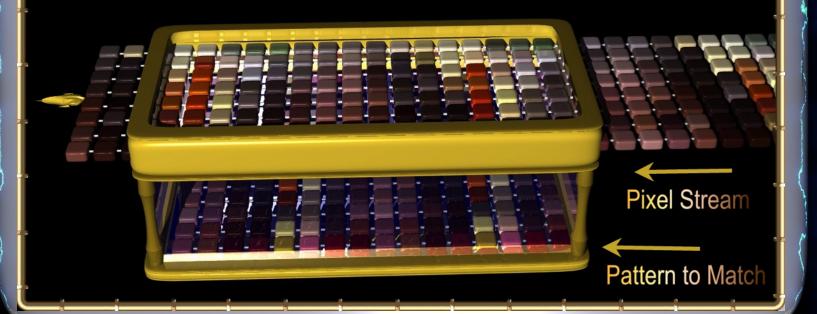
Cartesian to Polar Conversion:
 X = r.cos(φ), Y = r.sin(φ)
 one conversion / cycle.

Polar to Cartesian Conversion:
 r = √ X²+Y², φ=arccos(X /(√ X²+Y²))
 one conversion / cycle.



Motion Estimation & Pattern recognition MPEG 1....MPEG4

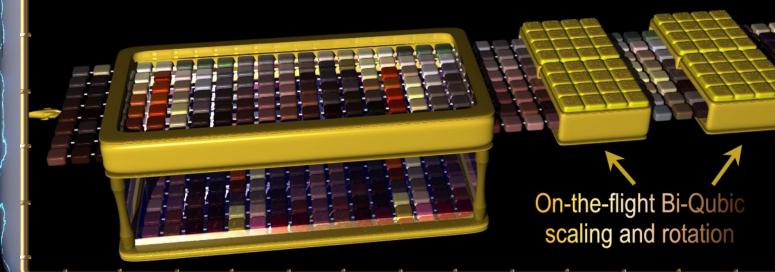
- Compares 128 8 bit pixels /cycle
- MxN kernel size up to 256 x 256
- Search window: 4096 x 4096
- Reduced Search Space Algorithms



# IIIIII GenTera MT processor

Motion Estimation,
Pattern recognition
in co-operation with
the Multipliers

- Half, quarter 1/8 and 1/16 pixels
- Arbitrary Scaling and Rotation
- High Quality Bi-Cubic Interpolation
- up to 120 million block compares/s



# (IIII) GenTera MT processor (IIII)

**Digital Video Decoding** 

Video Bit Stream Input





VLC Bitstream Decoder and Coefficient DeQuantizer

- Currently for MPEG 2,
- H.261 and MPEG 1
- Bit stream in / Coefficent out
- Next step is the DCT transform

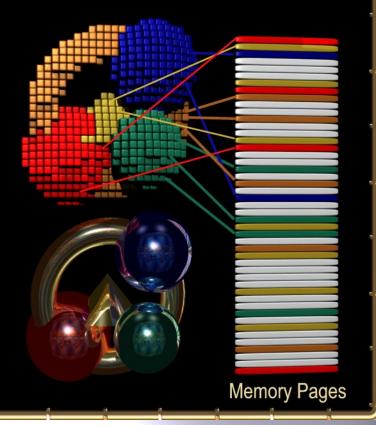
Select
Decode
Scan
Scale
Dequant.



Memory management: 1D, 2D and 3 Dimensional

Support for Virtual Memory Management uses 1D Pages, 2D Tiles and 3D Bricks.

- Simple Allocation and
- De-allocation
- High Memory Efficiency
- Optimizes DRAM access







Empty space doesn't waste Memory!

## GenTera MT processor Image Mask Generation Hardware Pixels written to Memory must pass the: The Polygon Mask The Window Mask The Depth Buffer Mask -----The Auxilary Mask for \_\_\_\_ various extra functions Supports the full Memory bus Bandwidth Presentation

#### GenTera MT processor High speed Dataflow ring for Inter Processor Stream communication, Point to Point or Broadcast GenTera GenTera GenTera GenTera MT3 MT3 MT3 MT3 GenTera GenTera GenTera GenTera MT3 MT3 MT3 MT3 Presentation

#### GenTera MT processor High End system design is enabled by the flexible I/O options Video Input Video Output High End System I/O GenTera GenTera GenTera GenTera MT3 MT3 MT3 MT3 I/O **FPGA** GenTera GenTera GenTera GenTera MT3 MT3 MT3 MT3 Presentation

# IIIII GenTera MT processor



**Future** 



Sony's Asimo

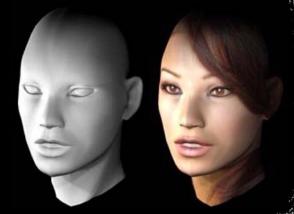


Future applications will use more real world inteligence

# 



3D Human Face Recognition



Reconstruction



Acqusition

High End applications are being developed today. Expected to grow to a billion chips/year market after 2012

# IIIIII GenTera MT processor IIIII



Face Recognition for Homeland Security





2005: Biometric chips in US Passports and Visa

# IIIIII GenTera MT processor IIIIIII



# IIIII GenTera MT processor

3D object match



Views generated with the Graphics Pipelines



and then matched with the "Motion Estimator" unit